Amendments to the Specification

Please add the following new paragraphs after page 5, line 2:

Fig. 9 is a voltage waveform diagram of gate lines according to a first embodiment of the present invention.

Fig. 10 is a voltage waveform diagram of gate lines according to first and second embodiments of the present invention.

Fig. 11 is a voltage waveform diagram of a gate line according to a third embodiment of the present invention.

Please replace the paragraphs on page 14, lines 7-13 with the following amended paragraphs:

As above, in each pixel row, gate lines GL and GL# are set to high voltage VGH in a select state, which can fully turn-on N-type TFT elements 16, 18 and 19 according to expression (6) in pixel 10#, so that maximum voltage VDHmax on data line DL is transmitted to pixel electrode node Np, as shown in Fig. 9. Fig. 9 illustrates that the voltage setting of gate lines GL and GL# in the select and non-select states.

In a non-select state, gate line GL is set to low voltage VGL, whereas gate line GL# is set to intermediate voltage VGM between high voltage VGH and low voltage VGL (VGH > VGM > VGL), as shown in Fig. 9.

Please replace the paragraph on page 18, lines 18-29 with the following amended paragraph:

Further, though the configuration example using N-type TFT elements 16, 18 and 19 are illustrated in Figs. 4 and 7, one or all of these TFT elements can be replaced by P-type TFT element(s) to form a pixel according to the first and second embodiments. In this case, the polarity of voltage setting of gate lines GL, GL# connected to the gate(s) of P-type TFT element(s) may be inverted. Specifically, low voltage VGL and high voltage VGH should be set to the voltages that can fully turn on/off the P-type TFT element(s) considering the transistor characteristics. Then, gate line GL should be driven to low voltage VGL in a select state and to high voltage VGH in a non-select state, while gate line GL# should be driven to low voltage VGL in a ~~non-select~~ select state and to intermediate voltage VGM in a non-select state, as shown in Fig. 10. Fig. 10 illustrates the voltage setting of gate lines GL and GL# in the select and non-select states when the P-type TFT elements are used.

Please replace the paragraph on page 19, lines 25-31 with the following amended paragraph:

By employing such a configuration, gate line driver 120 in a normal operation mode drives gate line GL# in a select state to high voltage VGH and drives gate line GL# in a non-select state to an intermediate voltage VGM, in response to a gate line select signal GSS. In a test mode, gate driver 120 drives gate line GL# in a select state to high voltage VGH and drives gate line GL# in a non-select state to low voltage VGL, similarly to gate line GL, in response to gate line select signal GSS, as shown in Fig. 11. Fig. 11 illustrates the voltage setting of gate line GL#.